WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a plurality of memory transistors;

a plurality of insulating layers disposed over the transistors;

a plurality of metal layers, each of the metal layers being disposed on one of the insulating layers; and

a plurality of metal plugs disposed over corresponding memory transistors, each of the metal plugs filling in a contact hole formed in one of the insulating layers and electrically connecting the metal layers disposed on a top side and a bottom side of the corresponding insulating layer,

wherein a top metal layer of the plurality of metal layers is configured to provide bit lines that correspond to the memory transistors, the metal plugs are vertically aligned, and one of the insulating layers is configured so that one of the memory transistors is connected to a corresponding bit line when a metal plug corresponding to said one of the memory transistors is provided in said one of the insulating layers.

2. The nonvolatile semiconductor memory device of claim 1, wherein the insulating layer configured for memory transistor connection is a top insulating layer of the plurality of the insulating layers.

3. The nonvolatile semiconductor memory device of claim 1, wherein a size of the metal plugs filling in the contact holes in a top insulating layer of the plurality of insulating layers is larger than a size of the metal plugs filling in the contact holes in an insulating layer of the plurality of insulating layers that is not the top insulating layer.

4. The nonvolatile semiconductor memory device of claim 2, wherein a size of the metal plugs filling in the contact holes in the top insulating layer is larger than a size of the

metal plugs filling in the contact holes in an insulating layer of the plurality of insulating layers that is not the top insulating layer.

5. A nonvolatile semiconductor memory device comprising:

a plurality memory transistors;

a first insulating layer disposed on the memory transistors;

a plurality of first metal plugs filling in contact holes formed in the first insulating layer, each of the memory transistors being connected to one of the first metal plugs;

a first metal layer disposed on the first metal plugs;

a second insulating layer disposed on the first metal layer;

a plurality of second metal plugs filling in contact holes formed in the second insulating layer, each of the first metal plugs being connected to one of the second metal plugs through the first metal layer;

a second metal layer disposed on the second metal plugs;

a third insulating layer disposed on the second metal layer; and

a third metal layer disposed on the third insulating layer and providing bit lines,

wherein a plurality of third metal plugs filling in contact holes formed in the third insulating layer are arranged so that one of the memory transistors is connected to a corresponding bit line when a third metal plug corresponding to said one of the memory transistors is provided in the third insulating layer, and the first metal plugs, the second metal plugs, the third metal plugs and the memory transistors are vertically aligned for the memory transistors that have corresponding third metal plugs.

6. A nonvolatile semiconductor memory device comprising:

a plurality memory transistors;

a first insulating layer disposed on the memory transistors;

a plurality of first metal plugs filling in contact holes formed in the first insulating layer, each of the memory transistors being connected to one of the first metal plugs;

a first metal layer disposed on the first metal plugs;

a second insulating layer disposed on the first metal layer;

a second metal layer disposed on the second insulating layer;

a third insulating layer disposed on the second metal layer;

a plurality of third metal plugs filling in contact holes formed in the third insulating layer, each of the third metal plugs being disposed on one of the memory transistors; and

a third metal layer disposed on the third metal plugs and providing bit lines,

wherein a plurality of second metal plugs filling in contact holes formed in the second insulating layer are arranged so that one of the memory transistors is connected to a corresponding bit line when a second metal plug corresponding to said one of the memory transistors is provided in the second insulating layer, and the first metal plugs, the second metal plugs, the third metal plugs and the memory transistors are vertically aligned for the memory transistors that have corresponding second metal plugs.

7. The nonvolatile semiconductor memory device of claim 5, wherein a size of the second metal plugs and a size of the third metal plugs are larger than a size of the first metal plugs.

8. The nonvolatile semiconductor memory device of claim 6, wherein a size of the second metal plugs and a size of the third metal plugs are larger than a size of the first metal plugs.